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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/238,262	01/27/1999	JOERG SCHAEFER	10191/955	6538

26646 7590 04/10/2002

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EXAMINER
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ART UNIT	PAPER NUMBER
1746	17

DATE MAILED: 04/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

T-P-17

Office Action Summary	Application No.	Applicant(s)	
	09/238,262	SCHAEFER ET AL.	
	Examiner	Art Unit	
	Anita K Alanko	1746	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10 and 12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. As to claim 10, although shown in the picture, the term "single material" is not explicitly described in the specification. This rejection may be overcome by amending the specification to include reference to a "single material." As to claim 12, the term "blind hole" is new matter, and it is unclear what a blind hole comprises.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The preamble cites that the method is for producing a micromechanical sensor arrangement, yet the body of the claim does not cite to form a micromechanical sensor arrangement. It is unclear how the method steps cited relate to forming a micromechanical sensor arrangement.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090) in view of Koide et al (U.S. Patent No. 5,389,198).

Iwasaki discloses a method (Fig. 15A-C) comprising the steps of:

- providing a wafer 30 having a surface and edge areas (Fig.15A);
- dividing the surface of the wafer into positive areas S2, to be subsequently etched in a wet chemical etching process, and negative areas (areas that are not to be etched) including the edge areas of the wafer;
- providing the negative areas with a passivation layer 33, 34 to protect the negative areas from the subsequent wet chemical etching process (Fig.15A, col.26, lines 12-15);
- etching the wafer in the wet chemical etching process (Fig.15B, col.26, lines 16-22); and

Iwasaki does not disclose to remove the passivation layer. Kiode teaches that it is conventional after etching, to remove the etch mask (Figures 6G', 7G', 8G'). It would have been obvious to one with ordinary skill in the art to remove the passivation layer in the method of Iwasaki because it is conventional to remove layers that are not required as a part of the final device, such as etch masks, as taught by Kiode.

As to claims 2-3, Iwasaki discloses in another embodiment to form a further mask 37 in at least subareas of the positive areas (Fig. 20, col.28, lines 24-26). Iwasaki does not disclose that the mask is a nitride layer since Iwasaki does not disclose the composition of the mask 37. Iwasaki discloses that the use of silicon nitride layers as masking layers is known (col.20, line

20). Iwasaki also discloses to use silicon nitride rather than silicon oxide layers because they can be formed to smaller thicknesses which improves processing etch times in aqueous KOH (col. 3, lines 53-65); It would have been obvious to one with ordinary skill in the art to use a nitride layer as the mask 37 in the method of Iwasaki to define part of the positive areas because Iwasaki teaches that they are conventional etch mask layers.

Iwasaki does not disclose how to structure the mask to form the pattern (Fig.19A,B). Examiner takes official notice that it is conventional in the art to pattern nitride layers by using a photoresist technique, such as an integrated circuit photoresist technique that uses exposing and developing steps. It would have been obvious to one with ordinary skill in the art to use a photoresist technique with exposing and developing to pattern nitride layer as a mask 37 in the method of Iwasaki because it is conventional in the art.

As to claim 4, Kiode teaches to form a series of masks, including nitride layers in subareas, 503, 504 (Fig.5), 603, 604 (Fig.6), and then removing them. It would have been obvious to one with ordinary skill in the art to apply a further passivation layer in the subareas and then remove them in the method of Iwasaki because Kiode teaches that this is a useful technique for forming three-dimensional structures in silicon.

As to claims 5-7, see the rejection of claims 2-3. Examiner takes official notice that it is conventional in the art to remove photoresist after patterning an underlying layer, such as a nitride layer. It would have been obvious to remove the photoresist after exposing and developing in the method of Iwasaki because it is conventional to remove a photoresist layer after patterning an underlying layer.

As to claim 8, Iwasaki discloses that the passivation layer 33, 34 is an oxide layer (col.26, lines 9-15).

As to claim 9, Iwasaki s discloses that the oxide layer is formed on the wafer (col.5, lines 24-25), but does not disclose that a LOCOS process is used. Examiner takes official notice that it is conventional in the art to form oxide layers by a LOCOS process. It would have been obvious to one with ordinary skill in the art to use a LOCOS process to form the oxide layer in the method of Iwasaki because it is a conventional technique for forming oxide layers.

Claims 1-9, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090) in view of Kiode et al (U.S. Patent No. 5,389,198) and O'Neill (U.S. Patent No. 5131978).

The discussion of modified Iwasaki from above is repeated here. ,

As to claim 4, Iwasaki does not disclose to apply a further passivation layer in subareas. O'Neill discloses a method for the fabrication of three dimensional structures from silicon comprising the steps of:

- providing a wafer 10 having a surface (Fig.3A);
- dividing the surface of the wafer into positive areas 20 (unmasked areas), to be subsequently etched in a wet chemical etching process, and negative areas (masked areas);
- providing the negative areas with a passivation layer 30, 32 to protect the negative areas from the subsequent wet chemical etching process (Fig.3A);
- etching the wafer in the wet chemical etching process (Fig.3D, col.5, line 53); and
- removing the passivation layer (Fig.3F, col.6, lines 25-27).

O'Neill discloses to divide the wafer into positive and negative areas by:

- applying a nitride layer 30 (col.5, line 5); and
- structuring the nitride layer 18 using a photoresist technique (col.5, line 11) so that the positive areas are defined by a part of the surface covered with the nitride layer;
- removing the nitride layer at least in subareas of the positive areas (where channel 20 is to be etched), after the negative areas are provided and before the wafer is etched (Fig.3B);
- applying a further passivation layer 38 (col.5, lines 26-28) in the subareas, after the removal of the nitride layer 30 in the subareas and before the wafer is etched; and
- completely removing the nitride layer (Fig.3F).

It would have been obvious to one with ordinary skill in the art to apply a further passivation layer and to remove the nitride layer in the method of Iwasaki as taught by O'Neill because O'Neill teaches that this is a conventional technique for patterning three dimensional structures in silicon by etching.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Burns et al (U.S. Patent No. 5,738,757) and Perng (U.S. Patent No. 6,033,997).

Burns discloses a method comprising:

- providing a wafer 10 having a surface and edge areas (Fig.1A);
- dividing the surface of the wafer into positive areas (unmasked areas in figures), to be subsequently etched in a wet chemical etching process, and negative areas (masked areas) including the edge areas of the wafer (since the figures show that edges are not etched);

- etching the wafer in the wet chemical etching process (col.5, line 8) to form various openings including caverns and through-holes (Fig.1I); and
- removing the passivation layers (Fig.1J).

Burns does not disclose providing the edge areas with a passivation layer. Perng teaches that during the processing and etching of a wafer, to protect the edges with a passivation layer 210, 270 (col.4, line 65-col.5, line 7). The layer that protects the edges is there throughout the processing to form the final product (Fig.1), which inherently requires etching steps. Therefore, it would have been obvious to one with ordinary skill in the art to provide the edge areas with a passivation layer in the method of Burns because Perng teaches that this provides additional protection at the bead region and sides of the wafer during etching of a silicon wafer.

As to claims 2-7, Burns discloses to form a series of passivation layers, including nitride layers in subareas that are structured by photoresist (Fig.1A-1J).

As to claims 8-9, Burns discloses that the passivation layer can be an oxide layer which is grown on the wafer (col.5, lines 21+). Burns does not explicitly disclose to use a LOCOS process. Examiner takes official notice that it is conventional in the art to form oxide layers by a LOCOS process. It would have been obvious to one with ordinary skill in the art to use a LOCOS process to form the oxide layer in the method of Burns because it is a conventional technique for forming oxide layers.

As to claims 10-13, Burns discloses to wet etch a single material, with varying size holes including caverns and through-holes (Fig.1A-1J).

Response to Amendment

The Renken rejections are withdrawn. Claims 10 and 12 are rejected under 35 U.S.C. 112, first paragraph. Claims 1-9, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090) in view of Koide et al (U.S. Patent No. 5,389,198). Claims 1-9, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090) in view of Kiode et al (U.S. Patent No. 5,389,198) and O'Neill (U.S. Patent No. 5131978). Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Burns et al (U.S. Patent No. 5,738,757) and Perng (U.S. Patent No. 6,033,997).

Response to Arguments

Applicant's arguments filed 2/11/02 are persuasive with respect to the Renken rejection.

As to the Iwasaki rejection, applicant argues about col.11, lines 36-45 of Iwasaki. However, this is from a different embodiment, Figure 1, than relied upon for the rejection. Even if it was the same embodiment, the argument "it is not the case that an oxide layer is selectively formed in exactly those areas (negative areas) which are not to be etch later" is not commensurate in scope with the claim language. The claim does not cite to selectively form anything.

Examiner acknowledges that Iwasaki does not teach to remove the passivation layer. Newly cited Kiode is cited to teach that removing passivation layers after etching is conventional.

Applicant argues that O'Neill does not teach to divide the surface into positive and negative areas. O'Neill does teach this, and so does Iwasaki. Processes that form etch masks inherently divide surfaces into those to be etched, and those not to be etched, i.e. "positive" and

"negative" areas. Etching patterns is inherently a predetermined process- to form a pattern, one must, out of necessity, decide beforehand what is to be etched, and what is not to be etched, which is equivalent to defining positive and negative areas.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pennell is cited to show a membrane that has been etched with no etch mask present in the final product. Harms is cited to show an etch mask on all sides of a wafer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K Alanko whose telephone number is 703-305-7708. The examiner can normally be reached on Monday-Friday,8:30 am-1:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Randy Gulakowski can be reached on 703-308-4333. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9057 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Anita K. Alanko
Primary Examiner
Art Unit 1746

AKA
April 8, 2002